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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/995,031	11/29/2001	Ricky Amos	YOR920010633US1 (062)	9669

7590 08/12/2002
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EXAMINER

LANDAU, MATTHEW C

ART UNIT	PAPER NUMBER
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2815

DATE MAILED: 08/12/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/995,031

Applicant(s)

AMOS ET AL.

Examiner

Matthew Landau

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-23 is/are pending in the application.
- 4a) Of the above claim(s) 17-23 is/are withdrawn from consideration.
- 5) ☐ Claim(s) ____ is/are allowed.
- 6) ☒ Claim(s) 1-16 is/are rejected.
- 7) ☐ Claim(s) ____ is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 29 November 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on ____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. ____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). ____
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) ____ 6) ☐ Other: ____

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DETAILED ACTION

Election/Restrictions

Applicant's election of Group I, device claims (claims 1-16) in Paper No. 4 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)). Therefore, claims 17-23 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in-

(1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or

(2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

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2. Claims 1-3, 5-12, and 14-16 are rejected under 35 U.S.C. 102(b) as being anticipated by Noguchi et al. (US Pat. 6,040,610, hereinafter Noguchi).

In regards to claim 1, Figure 23 of Noguchi discloses a MOS device comprising: a semi-conducting substrate 31 having source and drain regions 33; a gate dielectric layer 40 of less than 100 angstroms thickness (see column 24, lines 58-60) on said semi-conducting substrate 31; and a gate 41 formed of Pt (see column 46, lines 47-51) on top of said dielectric layer 40.

In regards to claim 2, Figure 23 of Noguchi discloses the gate dielectric layer 40 having a thickness less than 50 angstroms (see column 24, lines 58-60).

In regards to claim 3, Noguchi discloses the gate dielectric layer 40 is formed of SiO₂ (see column 23, lines 59-63).

In regards to claim 5, Noguchi discloses the gate dielectric layer 40 is formed of SiO₂ (see column 23, lines 59-63).

In regards to claim 6, Figure 23 of Noguchi discloses the semi-conducting substrate 31 has at least one source 33 and one drain 33.

In regards to claim 7, Figure 23 of Noguchi discloses the semi-conducting substrate 31 is p-type.

In regards to claim 8, Noguchi discloses the semi-conducting substrate 31 is formed of silicon (see column 23, lines 59-63).

In regards to claim 9, Noguchi discloses the semi-conducting substrate 31 is formed of silicon (see column 23, lines 59-63).

In regards to claim 10, Figure 23 of Noguchi discloses a FET comprising: a semi-conducting substrate 31 having source and drain regions 33; a gate dielectric layer 40 of less than

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100 angstroms thickness (see column 24, lines 58-60) on said semi-conducting substrate 31; and a gate 41 formed of Pt (see column 46, lines 47-51) on top of said dielectric layer 40.

In regards to claim 11, Figure 23 of Noguchi discloses the gate dielectric layer 40 having a thickness less than 50 angstroms (see column 24, lines 58-60).

In regards to claim 12, Noguchi discloses the gate dielectric layer 40 is formed of SiO₂ (see column 23, lines 59-63).

In regards to claim 14, Figure 23 of Noguchi discloses the semi-conducting substrate 31 is p-type.

In regards to claim 15, Noguchi discloses the semi-conducting substrate 31 is formed of silicon (see column 23, lines 59-63).

In regards to claim 16, Noguchi discloses the semi-conducting substrate is formed of silicon and the gate dielectric layer is SiO₂ (see column 23, lines 59-63).

3. Claims 1-4, and 6-15 are rejected under 35 U.S.C. 102(e) as being anticipated by Maria et al.

In regards to claim 1, Figure 4 of Maria et al. discloses a MOS device comprising: a semi-conducting substrate 16 having source 12 and drain 14 regions; a gate dielectric layer 20''' of less than 100 angstroms thickness (see page 3, paragraph [0033]) on said semi-conducting substrate 16; and a gate 22 formed of Pt (see page 3, paragraph [0034]) on top of said dielectric layer 20'''.

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In regards to claim 2, Figure 4 of Maria et al. discloses the gate dielectric layer 20''' having a thickness less than 50 angstroms (see page 3, paragraph [0033]).

In regards to claim 3, Figure 4 of Maria et al. discloses the gate dielectric layer 20''' is formed of a mixture of SiO_2 and a metal oxide.

In regards to claim 4, Figure 4 of Maria et al. discloses the gate dielectric layer 20''' is formed of La_2O_3 .

In regards to claim 6, Figure 4 of Maria et al. discloses the semi-conducting substrate 16 has at least one source 12 and one drain 14.

In regards to claim 7, Figure 4 of Maria et al. discloses the semi-conducting substrate 16 is n-type or p-type. It is inherent to have doped substrate in order to create a channel region below the gate.

In regards to claim 8, Maria et al. discloses the semi-conducting substrate 16 is formed of silicon (see page 3, paragraph [0033]).

In regards to claim 8, Maria et al. discloses the semi-conducting substrate 16 is formed of silicon (see page 3, paragraph [0033]).

In regards to claim 10, Figure 4 of Maria et al. discloses a FET comprising: a semi-conducting substrate 16 having source 12 and drain 14 regions; a gate dielectric layer 20''' of less than 100 angstroms thickness (see page 3, paragraph [0033]) on said semi-conducting substrate 16; and a gate 22 formed of Pt (see page 3, paragraph [0034]) on top of said dielectric layer 20'''.

In regards to claim 11, Figure 4 of Maria et al. discloses the gate dielectric layer 20''' having a thickness less than 50 angstroms (see page 3, paragraph [0033]).

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In regards to claim 12, Figure 4 of Maria et al. discloses the gate dielectric layer 20''' is formed of a mixture of SiO_2 and a metal oxide.

In regards to claim 13, Figure 4 of Maria et al. discloses the gate dielectric layer 20''' is formed of La_2O_3 .

In regards to claim 14, Figure 4 of Maria et al. discloses the semi-conducting substrate 16 is n-type or p-type. It is inherent to have doped substrate in order to create a channel region below the gate.

In regards to claim 15, Maria et al. discloses the semi-conducting substrate 16 is formed of silicon (see page 3, paragraph [0033]).

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Inumiya et al. discloses a p-type silicon substrate with source and drain regions, a gate dielectric formed of SiO_2 with a thickness less than 50 angstroms, and an Ru gate electrode. Numata et al. discloses an SOI substrate with source and drain regions, a gate dielectric formed of SiO_2 with a thickness less than 50 angstroms, and a platinum gate electrode.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew C. Landau whose telephone number is (703) 305-4396.

The examiner can normally be reached on 8:00 AM-4: 30 PM.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (703) 308-1690. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.


ALLAN R. WILSON
PRIMARY EXAMINER

Matthew C. Landau

Examiner

August 8, 2002